

DESCRIPTIONS

The SN74LVC1G02 single 2-input positive-NOR gate is designed for 1.65V to 5.5V V_{CC} operation.

The SN74LVC1G02 device performs the Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \cdot \overline{B}$ in positive logic. The device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The SN74LVC1G02 is available in Green SOT23-5 and SC70-5 packages. It operates over an ambient temperature range of -40°C to +125°C.

FEATURES

- **Operating Voltage Range: 1.65V to 5.5V**
- **Low Power Consumption: 0.1μA (TYP)**
- **Operating Temperature Range:**
-40°C to +125°C
- **Inputs Accept Voltage to 5.5V**
- **High Output Drive: ±24mA at $V_{CC}=3.0V$**
- **Micro SIZE PACKAGES: SOT23-5, SC70-5**

APPLICATIONS

- **Active Noise Elimination**
- **Bar Code Scanner**
- **Blood Pressure Monitor**
- **CPAP Machine**
- **Fingerprint identification**
- **Network attached storage (NAS)**

PACKAGE/ORDERING INFORMATION ⁽¹⁾

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING ⁽²⁾	MSL ⁽³⁾	PACKAGE OPTION
SN74LVC1G02	SN74LVC1G02DCKR	-40°C ~+125°C	SC70-5 ⁽⁴⁾	ICBK	MSL3	Tape and Reel,3000
	SN74LVC1G02DBVR	-40°C ~+125°C	SOT23-5	C02J	MSL3	Tape and Reel,3000

NOTE:

- (1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document.
- (2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.
- (3) MSL, The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications.
- (4) Equivalent to SOT353.

SIMPLIFIED SCHEMATIC



FUNCTION TABLE

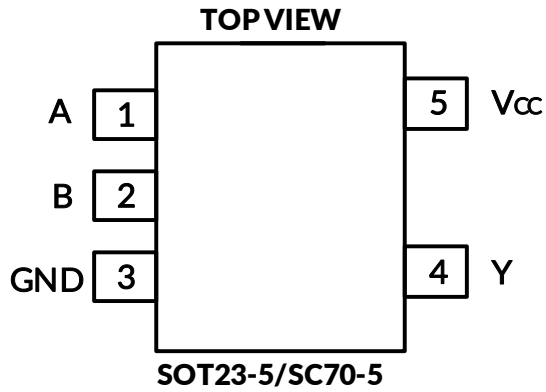
INPUTS		OUTPUT
A	B	Y
H	H	L
L	H	L
H	L	L
L	L	H

$$Y = \overline{A + B}$$

H=High Voltage Level

L=Low Voltage Level

PIN CONFIGURATION AND FUNCTIONS (TOP VIEW)



PIN	NAME	I/O	FUNCTION
1	A	I	Input
2	B	I	Input
3	GND	P	Ground
4	Y	O	Output
5	V _{CC}	P	Power pin

REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
Rev A.1	2026/01/09	Initial version completed

Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	6.5	V
V _I	Input voltage range ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	-0.5	V _{CC} +0.5	V
I _{IK}	Input clamp current	V _I <0		-50 mA
I _{OK}	Output clamp current	V _O <0		-50 mA
I _O	Continuous output current			±50 mA
Continuous current through V _{CC} or GND				±100 mA

Package Thermal Impedance

PARAMETER		MIN	MAX	UNIT
θ _{JA}	Package thermal impedance ⁽⁴⁾	SOT23-5	230	°C/W
		SC70-5	380	

Temperature

PARAMETER		MIN	MAX	UNIT
Temperature	Junction temperature, T _J ⁽⁵⁾	-65	150	°C
	Storage temperature, T _{stg}	-65	150	

ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

	VALUE	UNIT	 ESD SENSITIVITY CAUTION ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.
Human-Body Model (HBM)	±2000	V	
Charged-Device Model (CDM)	±1000		
Machine Model (MM)	±200		

NOTE:

- Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- The value of V_{CC} is provided in the Recommended Operating Conditions table.
- The package thermal impedance is calculated in accordance with JEDEC-51.
- The maximum power dissipation is a function of T_{J(MAX)}, R_{θJA}, and T_A. The maximum allowable power dissipation at any ambient temperature is P_D = (T_{J(MAX)} - T_A) / R_{θJA}. All numbers apply for packages soldered directly onto a PCB.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range (TYP values are at $T_A = +25^{\circ}\text{C}$, Full= -40°C to 125°C , unless otherwise noted.) ⁽¹⁾

Recommended Operating Conditions

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage	V_{CC}	Operating	1.65	5.5	V
		Data retention only	1.5		
High-level input voltage	V_{IH}	$V_{CC}=1.65\text{V to }1.95\text{V}$	$0.65 \times V_{CC}$		V
		$V_{CC}=2.3\text{V to }2.7\text{V}$	1.7		
		$V_{CC}=3\text{V to }3.6\text{V}$	2		
		$V_{CC}=4.5\text{V to }5.5\text{V}$	$0.7 \times V_{CC}$		
Low-level input voltage	V_{IL}	$V_{CC}=1.65\text{V to }1.95\text{V}$		$0.35 \times V_{CC}$	V
		$V_{CC}=2.3\text{V to }2.7\text{V}$		0.7	
		$V_{CC}=3\text{V to }3.6\text{V}$		0.8	
		$V_{CC}=4.5\text{V to }5.5\text{V}$		$0.3 \times V_{CC}$	
Input voltage	V_I		0	5.5	V
Output voltage	V_O		0	V_{CC}	V
Input transition rise or fall	$\Delta t / \Delta v$	$V_{CC}=1.8\text{V} \pm 0.15\text{V}, 2.5\text{V} \pm 0.2\text{V}$		20	ns/V
		$V_{CC}=3.3\text{V} \pm 0.3\text{V}$		10	
		$V_{CC}=5\text{V} \pm 0.5\text{V}$		5	
Operating temperature	T_A		-40	125	$^{\circ}\text{C}$

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

DC Characteristics

PARAMETER	TEST CONDITIONS	V _{CC}	TEMP	MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
V _{OH}	I _{OH} = -100μA	1.65V to 5.5V		V _{CC} -0.1			
	I _{OH} = -4mA	1.65V		1.2			
	I _{OH} = -8mA	2.3V		1.9			
	I _{OH} = -16mA		Full	2.4			V
	I _{OH} = -24mA	3V		2.3			
	I _{OH} = -32mA	4.5V		3.8			
V _{OL}	I _{OL} = 100μA	1.65V to 5.5V				0.1	
	I _{OL} = 4mA	1.65V				0.45	
	I _{OL} = 8mA	2.3V				0.3	
	I _{OL} = 16mA		Full			0.4	V
	I _{OL} = 24mA	3V				0.55	
	I _{OL} = 32mA	4.5V				0.55	
I _I	A or B inputs	V _I =5.5V or GND	0V to 5.5V	+25°C Full	±0.1	±5	μA
I _{off}		V _I or V _O =5.5V	0	+25°C Full	±0.1	±10	μA
I _{CC}		V _I =5.5V or GND, I _O =0	1.65V to 5.5V	+25°C Full	0.1	10	μA
ΔI _{CC}		One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND	3V to 5.5V	Full		500	μA
C _i (Input Capacitance)		V _I =V _{CC} or GND	3.3V	+25°C		4	pF

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

(2) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.

(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

AC Characteristics

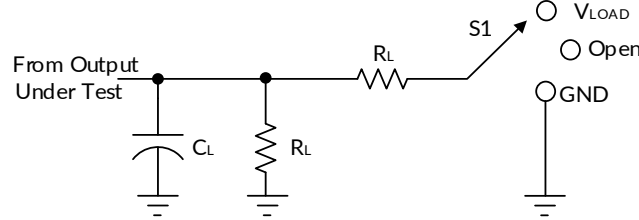
PARAMETER	SYMBOL	TEST CONDITIONS	MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
Propagation Delay	t _{pd}	V _{CC} =1.8V±0.15V C _L =30pF, R _L =1kΩ		13.3		
		V _{CC} =2.5V±0.2V C _L =30pF, R _L =500Ω		5.3		
		V _{CC} =3.3V±0.3V C _L =50pF, R _L =500Ω		4.1		ns
		V _{CC} =5V±0.5 V C _L =50pF, R _L =500Ω		3.6		
Power dissipation capacitance	C _{pd}	V _{CC} =1.8V		16		
		V _{CC} =2.5V		18		
		V _{CC} =3.3V	f=10MHz	18		pF
		V _{CC} =5V		20		

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

(2) This parameter is ensured by design and/or characterization and is not tested in production.

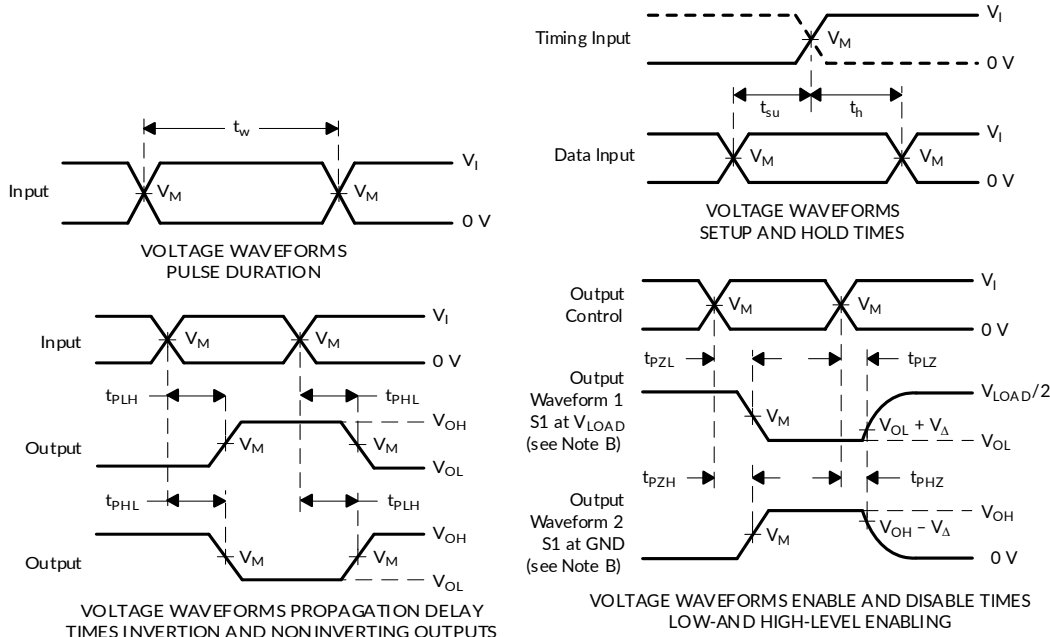
(3) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.

PARAMETER MEASUREMENT INFORMATION



TEST			S1				
t_{PLH}/t_{PHL}			Open				
t_{PLZ}/t_{PZL}			V_{LOAD}				
t_{PHZ}/t_{PZH}			GND				

INPUTS							
V_{CC}	V_I	t_r/t_f	V_M	V_{LOAD}	C_L	R_L	V_{Δ}
1.8V±0.15V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	30pF	1kΩ	0.15V
2.5V±0.2V	V_{CC}	≤2ns	$V_{CC}/2$	2 x V_{CC}	30pF	500Ω	0.15V
3.3V±0.3V	3V	≤2.5ns	1.5V	6V	50pF	500Ω	0.3V
5V±0.5V	V_{CC}	≤2.5ns	$V_{CC}/2$	2 x V_{CC}	50pF	500Ω	0.3V



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.

Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O = 50\Omega$.

D. The outputs are measured one at a time, with one transition per measurement.

E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .

F. t_{PZL} and t_{PZH} are the same as t_{en} .

G. t_{PLH} and t_{PHL} are the same as t_{pd} .

H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

DETAILED DESCRIPTION

Overview

The SN74LVC1G02 device contains one 2-input positive-NOR gate and performs the Boolean function $Y = \overline{A + B}$ or $Y = \overline{A} \cdot \overline{B}$. This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Functional Block Diagram



Feature Description

- Wide operating voltage range.
 - Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- I_{off} feature allows voltages on the inputs and outputs, when V_{CC} is 0 V.

APPLICATION AND IMPLEMENTATION

Application Information

The SN74LVC1G02 is a high drive CMOS device that can be used for implement NOR logic with a high output drive, such as an LED application. It can produce 24mA of drive current at 3.0V making it Ideal for driving multiple outputs and good for high speed applications up to 100MHz. The inputs are 5.5V tolerant allowing translation down to V_{CC} .

Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

POWER SUPPLY RECOMMENDATIONS

The power supply pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a $0.1\mu\text{F}$ capacitor is recommended and if there are multiple V_{CC} terminals then $0.01\mu\text{F}$ or $0.022\mu\text{F}$ capacitors are recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The $0.1\mu\text{F}$ and $1\mu\text{F}$ capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible.

LAYOUT

Layout Guidelines

When using multiple bit logic devices inputs should not ever float. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally, they will be tied to GND or V_{CC} whichever make more sense or is more convenient.

Layout Example

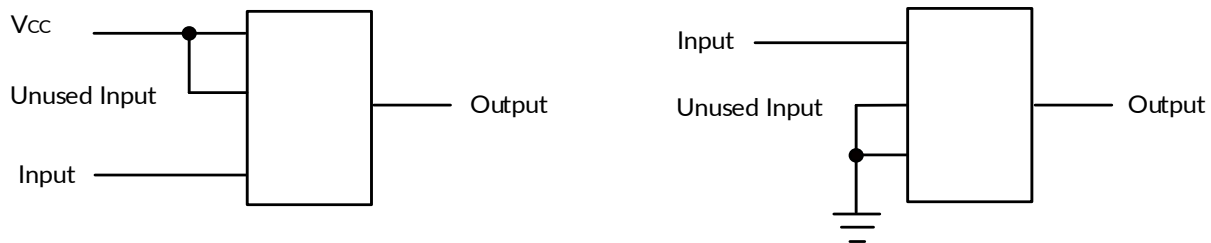
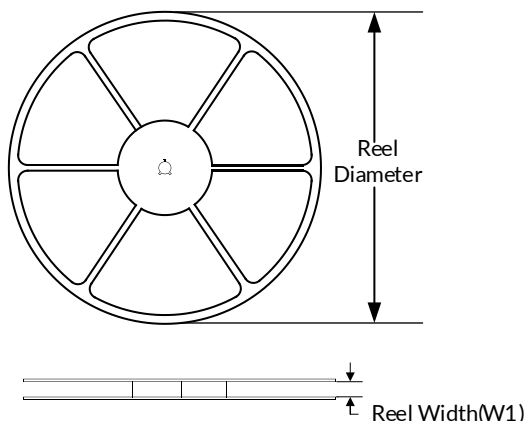


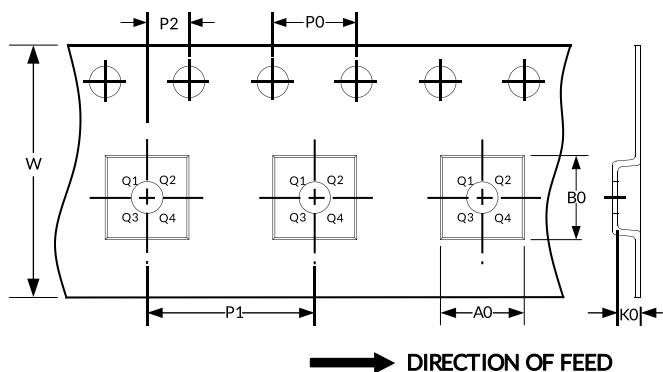
Figure 2. Layout Diagram

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSION



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
SC70-5	7"	9.5	2.25	2.55	1.20	4.0	4.0	2.0	8.0	Q3
SOT23-5	7"	9.5	3.20	3.20	1.40	4.0	4.0	2.0	8.0	Q3

NOTE:

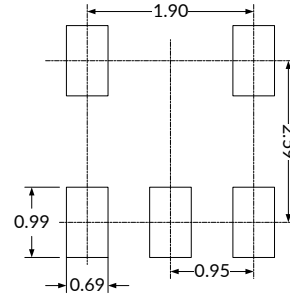
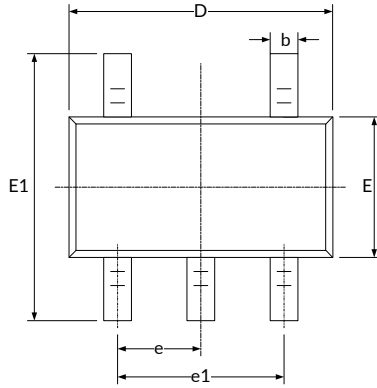
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

PACKAGE OUTLINE DIMENSIONS

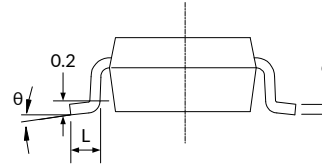
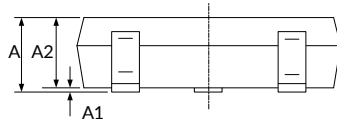
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

SOT23-5 ⁽³⁾



RECOMMENDED LAND PATTERN (Unit: mm)

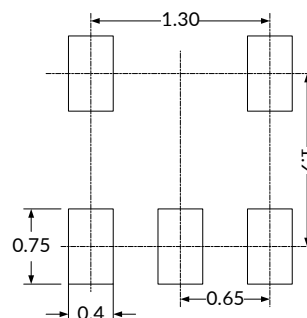
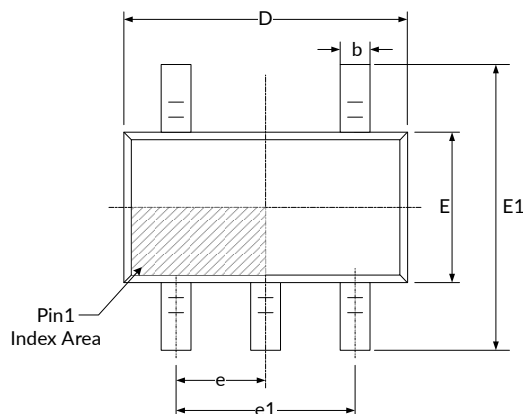


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A ⁽¹⁾	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D ⁽¹⁾	2.820	3.020	0.111	0.119
E ⁽¹⁾	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC) ⁽²⁾		0.037(BSC) ⁽²⁾	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

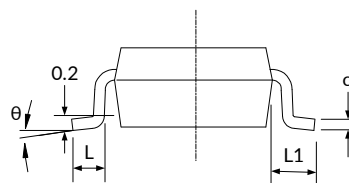
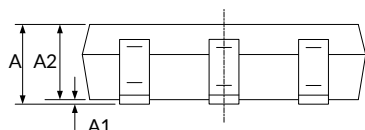
NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. REF is the abbreviation for Reference.
3. This drawing is subject to change without notice.

SC70-5⁽³⁾



RECOMMENDED LAND PATTERN (Unit: mm)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A ⁽¹⁾	0.900	1.100	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.000	0.035	0.039
b	0.150	0.350	0.006	0.014
c	0.110	0.175	0.004	0.007
D ⁽¹⁾	2.000	2.200	0.079	0.087
E ⁽¹⁾	1.150	1.350	0.045	0.053
E1	2.150	2.450	0.085	0.096
e	0.650(TYP)		0.026(TYP)	
e1	1.200	1.400	0.047	0.055
L	0.260	0.460	0.010	0.018
L1	0.525(REF) ⁽²⁾		0.021(REF) ⁽²⁾	
θ	0°	8°	0°	8°